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| 10/538,563   | 06/15/2005  | Edwin Rijpkema       | NL021330            | 9446             |
| 65913  | 7590        | 06/11/2009           | EXAMINER            |                  |
| NXP, B.V.<br>NXP INTELLECTUAL PROPERTY & LICENSING<br>M/S41-SJ<br>1109 MCKAY DRIVE<br>SAN JOSE, CA 95131 |             |                      | KAO, JUTAI          |                  |
|  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2416                |                  |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

|                              |                                      |  |  |
|------------------------------|--------------------------------------|--|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/538,563 | <b>Applicant(s)</b><br>RIJPKEMA, EDWIN |  |
|                              | <b>Examiner</b><br>JUTAI KAO         | <b>Art Unit</b><br>2416                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,4-6,9-16 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-6,9-16 and 19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

***Oath/Declaration***

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/30/2009 has been entered.

***Response to Amendment***

Amendments filed on 03/30/2009 change the scope of the previous claims, rendering previous grounds of rejections moot. New grounds of rejections are applied in the current office action.

Claims 5-6 and 9-10 were not addressed in the applicant's remark as claim 5 is an independent claim in itself and claims 6 and 9-10 depends on claim 5. Also, claim 5 was previously amended in the amendment filed on 02/01/2008, thus should be labeled as (previously presented) instead of (Original).

***Response to Arguments***

2. Applicant's arguments with respect to claims 1, 4-6, 9-16 and 19-21 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 1, the applicant argues that previous rejections do not show the amended features of "at least one guaranteed throughput input buffer selectively coupled to at least one data switch input by the combined control means". Specifically, as previously shown, Moore discloses coupling of the guaranteed throughput input buffer to at least one data switch input, but fails to disclose the selective coupling as currently claimed. In response, a previously cited reference, Dell (US 2002/0085578) shows in Fig. 10, wherein a plurality of input buffers (as shown in the 1<sup>st</sup> stage block) are selectively coupled to the switch (as shown as the 2<sup>nd</sup> stage block) by a selector (represented as a circled "S" in the 1<sup>st</sup> stage block).

Regarding claim 11, the applicant argues that previous rejections do not show the amended features of "best effort control means to selectively fill said best effort input buffers with best effort data and schedule the best effort data for transfer through the switching matrix, wherein best effort control means is further configured to schedule the best effort data based on a contention free guaranteed throughput scheduling". Specifically, previous rejection does not include the selective filling of said best effort input buffers. In response, Dell shows the selective filling of buffers as shown in step 2 of Fig. 10. Thus, when combined with Chiussi, which shows filling best effort input queues with best effort traffic, the claimed limitation of selectively filling best effort input buffers with best effort data is anticipated by the combination. Dell also discloses having queues of different priority and destinations, wherein priority level includes best-effort traffic (see paragraph [0105]), thus making this combination obvious.

Regarding both claims 1 and 11, the applicant argues that previous rejection does not show the step of “reserving a GT connection input to any output of the data switch so that no BE data is sent to the same data switch input as the GT data to simplify the BE scheduling” (see page 14, point 3 of the applicant’s remark). However, such feature is not found in claims 1 or 11. Therefore, the argument is not persuasive.

### ***Claim Objections***

3. Claims 1, 4, 11-16 and 19-21 are objected to because of the following informalities: grammatical error.

Regarding claim 1, line 11-13 recites “wherein the one step comprises at least a one of a reservation of a least one data...”, wherein the underlined portion is redundant.

Regarding claim 11, line 12 recites “wherein the one step comprises at least a one of a reservation of at least...”, wherein the underlined portion is redundant.

Claims 4, 11-16 and 19-21 are objected to due to their dependencies on claims 1 or 11.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi (US 2003/0142624) in view of Moore (US 2004/0136370) and Dell (US 2002/0085578).

Chiussi discloses a method for integrating guaranteed-bandwidth and best-effort traffic in a packet network including the following features.

Regarding claim 1, a data switching device (see device 101-1 in Fig. 2) comprising an incoming stream of guaranteed throughput data (see Flow gb1 402 in Fig. 4); an incoming stream of best effort data (see flow be1 405 in Fig. 4); data switch inputs (see input links 201-1 to 201-s in Fig. 2) for guaranteed throughput and best effort data (see Fig. 5, which shows the incoming Guaranteed Bandwidth (GB) flows 402 and Best Effort (BE) flows 405); data switch outputs (see output links 204 by the switch fabric 250 in Fig. 2), a data switch interconnecting the data switch inputs and data switch outputs (see data switch 101-1, switching via the I/O switch fabric 250 in Fig. 2), combined control means (see combined scheduling means shown in Fig. 4) for controlling data scheduling of the incoming streams to the data switch such that the best effort data scheduling is based on a contention free guaranteed throughput scheduling (see “serves the BE aggregate only after having granted to the GB aggregate the sum of the guaranteed service shares of the allocated GB flows” recited in paragraph [0040]); guaranteed throughput control means coupled for controlling a guaranteed throughput data scheduling (see PWS 401 in Fig. 4) to schedule the guaranteed data in one step (see Fig. 4, where the GB flows gets scheduled by only going through the PWS scheduling step 401), wherein the one step comprises at least a one of a

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reservation of at least one data switch input and a reservation of at least one data switch output (see Fig. 4, where the PWS puts the GB flow within the subframe 407, and sending the frame to the outgoing link, thus reserving an output link for the GB flow), and best effort control means coupled for controlling a best effort data scheduling (see SWS 404 in Fig. 4); and at least one guaranteed throughput input buffer coupled to at least one data switch input (see flow queues 502 in Fig. 5) by the combined control means; wherein the at least one guaranteed throughput input buffer is configured to store only one unit of guaranteed throughput data at a time (see Fig. 5, where each flow queue 502 only carries one GB flow).

Regarding claim 4, wherein the data-switching device has one and the same output buffer both for collecting guaranteed throughput and best effort data (see packet RAM 607 in Fig. 6, which carries all packets to be transmitted by the packet transmitter 601, including both the GB and BE flows, as recited in paragraph [0048]).

Chiussi does not specifically disclose the following features: regarding claims 1, wherein the guaranteed throughput scheduling is contention free; and wherein at least one guaranteed throughput input buffer is **selectively** coupled to the at least one data switch input by the combined control means.

Moore discloses a system for per flow guaranteed throughput, multiple TCP flow bandwidth provisioning including the following features.

Regarding claims 1, wherein the guaranteed throughput scheduling is contention free (see guaranteed throughput...eliminates...contention" recited in paragraph [0004]).

Dell discloses a three-stage switch fabric with buffered crossbar devices including the following features.

Regarding claim 1, wherein at least one guaranteed throughput input buffer is ***selectively*** coupled to the at least one data switch input by the combined control means (see Fig. 10, wherein the input buffers, which may include guaranteed throughput input buffers as shown by Chiussi and mentioned in paragraph [0106] of Dell, in the 1<sup>st</sup> stage block being selectively connected to the 2<sup>nd</sup> switch crossbar switch by the selector/scheduler shown as the circled “S” in the 1<sup>st</sup> stage block; as for the example of Fig. 10, the second queue is currently being selected).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Chiussi using features, as taught by Moore, in order to provide “bandwidth, throughput, and/or goodput provisioning of multiple TCP flows across shared links” and to obviate “the need for congestion signaling” (see Moore, paragraph [0004]) and in order to provide scheduling based on the QoS (see “Queue Structures, QoS Schedulers” section under paragraph [0105] of Dell).

6. Claims 5-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi (US 2003/0142624) in view of Moore (US 2004/0136370).

Chiussi discloses a method for integrating guaranteed-bandwidth and best-effort traffic in a packet network including the following features.

Regarding claim 5, a data switching method (see switch fabric 250 in Fig. 2), comprising: scheduling, in one step (see Fig. 4, where the GB flows gets scheduled by

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only going through the PWS scheduling step 401), guaranteed throughput data for switching (see Fig. 4, which schedules both GB and BE flows using primary and secondary weighted-round-robin schedulers (PWS and SWS) 401 and 404), wherein the one step comprises a reservation of inputs and/or outputs (see Fig. 4, where the PWS puts the GB flow within the subframe 407, and sending the frame to the outgoing link, thus reserving an output link for the GB flow); and scheduling best effort data for switching, wherein the best effort data scheduling is based on a contention free guaranteed data scheduling (see “serves the BE aggregate only after having granted to the GB aggregate the sum of the guaranteed service shares of the allocated GB flows” recited in paragraph [0040]).

Regarding claim 6, characterized in that the best effort scheduling is performed after the guaranteed throughput scheduling (see “serves the BE aggregate only after having granted to the GB aggregate the sum of the guaranteed service shares of the allocated GB flows” recited in paragraph [0040]; or see “first...the PWS 401 fulfills the bandwidth requirements of the GB flows” and “second...the PWS 401 distributes fair service to the plurality of BE flows” recited in paragraph [00043]).

Regarding claim 9, wherein the best effort data scheduling takes one or more multiples of three steps, including the steps: request, grant and accept (see “the single WRR scheduler grants 0.66 r to the GB flow that remains backlogged, while each BE flow gets 1.66% of the capacity of the server...” recited in paragraph [0039], which shows how the WRR scheduler grants 1.66% of the capacity to the BE flows).

Chiussi does not specifically disclose the following features: regarding claim 5, wherein the guaranteed throughput scheduling is contention free.

Moore discloses a system for per flow guaranteed throughput, multiple TCP flow bandwidth provisioning including the following features.

Regarding claim 5, wherein the guaranteed throughput scheduling is contention free (see guaranteed throughput...eliminates...contention" recited in paragraph [0004]).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Chiussi using features, as taught by Moore, in order to provide "bandwidth, throughput, and/or goodput provisioning of multiple TCP flows across shared links" and to obviate "the need for congestion signaling" (see Moore, paragraph [0004]).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi (US 2003/0142624) in view and Moore (US 2004/0136370) as applied to claim 9 above, and further in view of Hill (US 2003/0035422).

Chiussi in view of Moore disclose the claimed limitations as described above.

Chiussi and Moore do not disclose the following features: regarding claim 9, wherein a contention resolution for said best effort data scheduling is based on bipartite graph matching.

Hill discloses a packet switching method including the following features.

Regarding claim 10, wherein a contention resolution for said best effort data scheduling is based on bipartite graph matching (see "scheduling of connectionless,

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best-effort packets ...based on maximum size and maximum weight bipartite graph matching algorithms” as recited in paragraph [0003]).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to further modify the system of Chiussi and Moore using features, as taught by Hill, in order to create conflict-free connections between inputs and outputs of each timeslot (recited in Hill, paragraph [0003]).

8. Claims 11-16 and 19-21 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Karawai (US 2001/0033581) in views of Chiussi, Moore and Dell.

Karawai discloses a packet switch, scheduling device, drop control circuit, multicast control circuit and QoS control device including the following features.

Regarding claim 11, a data switching device (see device shown in Fig. 1 and 4): a switching matrix to switch data from a plurality of inputs to a plurality of outputs (see switch 16 in Fig. 1); a plurality of multiplexers coupled to the plurality of inputs of the switching matrix (see multiplexer in the plurality of input buffer sections 12, which is connected to the matrix switch 16 as shown in Fig. 4); a plurality of best effort input buffers coupled as inputs to the plurality of multiplexers, each of the best effort input buffers to store best effort data (see Fig. 6, bottom queue within input buffer section 12 carries best effort class traffic); a guaranteed throughput input buffer coupled as another input to a first multiplexer of the plurality of multiplexers, the guaranteed throughput input buffer to store guaranteed throughput data (see Fig. 6, top queue within input buffer section 12 carries band guaranteed class traffic); and combined scheduling

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means coupled to the plurality of multiplexers (see scheduling sections 25 connected to the multiplexers, as shown in Fig. 4), the combined scheduling control means comprising: guaranteed throughput control means and best effort control means (see the scheduling and selected line management in scheduler section 25 connected separately to the bandwidth guaranteed traffic and the best effort traffic).

Regarding claim 12, a plurality of output buffers coupled to the plurality of outputs of the switching matrix (see output buffers 18 connected to the output of the switching matrix 16, as shown in Fig. 1), wherein each output buffer is configured to collect both guaranteed throughput and best effort data (see output buffer 18 accepting data of QoS 1-4 in Fig 1, wherein the QoS classes 1-4 include band guaranteed class and best effort class).

Karawai does not explicitly disclose the following features: regarding claim 11, wherein the combined scheduling control means comprises: guaranteed throughput control means to schedule the guaranteed throughput data in one step, wherein the one step comprises at least a one of a reservation of at least one data switch input and a reservation of at least one data switch output, for transfer through the switching matrix to one of the plurality of outputs of the switching matrix; and best effort control means to schedule the best effort data fort transfer through the switching matrix to another one of the plurality of outputs of the switching matrix, wherein the best effort control means to selectively fill said best effort input buffers with best effort data and schedule the best effort data based on a contention free guaranteed throughput scheduling; regarding claim 13, wherein the guaranteed throughput input buffer is configured to store only one

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unit of guaranteed throughput data at a time; regarding claim 14, wherein the best effort control means is further configured to disable best effort requests corresponding to the input of the switching matrix to which the first multiplexer is coupled for a frame during which the guaranteed throughput data is transferred through the switching matrix; regarding claim 15, wherein the best effort control means is further configured to disable best effort requests corresponding to the output of the switching matrix to which the guaranteed throughput data is transferred for a frame during which the guaranteed throughput data is transferred through the switching matrix; regarding claim 16, wherein the best effort control means is further configured to schedule the best effort data after the guaranteed throughput control means schedules the guaranteed throughput data; regarding claim 19, wherein the best effort control means is further configured to schedule the best effort data and three steps, wherein the three steps comprises a request step, a grant step, and an accept step; regarding claim 20, wherein the best effort control means is further configured to schedule the best effort data using multiples of the three steps; regarding claim 21, the data switching device further comprises a plurality of demultiplexers coupled to the plurality of best effort input buffers, wherein a first demultiplexer of the plurality of demultiplexers is also coupled to guaranteed throughput input buffer, wherein the first demultiplexer is configured to distribute data from an incoming data stream to a corresponding best effort input buffer or the guaranteed throughput input buffer; Chiussi discloses a method for integrating guaranteed-bandwidth and best-effort traffic in a packet network including the following features

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Regarding claim 11, guaranteed throughput control means (see PWS 401 in Fig. 4) to schedule the guaranteed throughput data in one step, wherein the one step (see Fig. 4, where the GB flows gets scheduled by only going through the PWS scheduling step 401), wherein the one step comprises at least a one of a reservation of at least one data switch input and a reservation of at least one data switch output (see Fig. 4, where the PWS puts the GB flow within the subframe 407, and sending the frame to the outgoing link, thus reserving an output link for the GB flow), for transfer (see flow gb1-gbV 402 in Fig. 4) through the switching matrix (see switch fabric 250 in Fig. 2) to one of the plurality of outputs of the switching matrix (see link 204 connecting to the communication link interface 200-j); and best effort control means (see SWS 404 in Fig. 4) to schedule the best effort data (see Flow be1-beU 405 in Fig. 4) for transfer through the switching matrix (see switch fabric 250 in Fig. 2) to another one of the plurality of outputs of the switching matrix (see link 204 connecting to the communication link interface 200-s; that is, the schedulers shown in Fig. 4 are part of the communication link interfaces 200-1 through 200-i, as shown in Fig. 6; and as shown in Fig. 4, each of the scheduler outputs frames including both the guaranteed flow and the best effort flow; the outputs of the communication link interfaces are then sent to the switch fabric 250 and output to the plurality of outputs of the switch fabric, shown by links 204, since each of these outputs include both the guaranteed flow and the best effort flows, therefor, the guaranteed throughput data is transfer to one of the plurality of outputs of the switching matrix and the best effort data is transfer to the same output of the switching matrix as well as all other outputs of the switching matrix), wherein the best

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effort control means is further configured to schedule the best effort data based on a contention free guaranteed throughput scheduling (see “serves the BE aggregate only after having granted to the GB aggregate the sum of the guaranteed service shares of the allocated GB flows” recited in paragraph [0040]).

Regarding claim 13, wherein the guaranteed throughput input buffer is configured to store only one unit of guaranteed throughput data at a time (see Fig. 5, where each flow queue 502 only carries one GB flow).

Regarding claim 16, characterized in that the best effort scheduling is performed after the guaranteed throughput scheduling (see “serves the BE aggregate only after having granted to the GB aggregate the sum of the guaranteed service shares of the allocated GB flows” recited in paragraph [0040]; or see “first...the PWS 401 fulfills the bandwidth requirements of the GB flows” and “second...the PWS 401 distributes fair service to the plurality of BE flows” recited in paragraph [00043]).

Regarding claim 21, the data switching device further comprises a plurality of demultiplexers (see demultiplexers in input buffer sections 12 in Fig. 4) coupled to the plurality of best effort input buffers, wherein a first demultiplexer of the plurality of demultiplexers is also coupled to guaranteed throughput input buffer, wherein the first demultiplexer is configured to distribute data from an incoming data stream to a corresponding best effort input buffer or the guaranteed throughput input buffer (see demultiplexer in Fig. 4, which distributes data into the queue sections 0-M and as shown in Fig. 6, divide the data into band guaranteed class and the best effort class).

Moore discloses a system for per flow guaranteed throughput, multiple TCP flow bandwidth provisioning including the following features.

Regarding claims 11, wherein the guaranteed throughput scheduling is contention free (see guaranteed throughput...eliminates...contention” recited in paragraph [0004]).

Dell discloses a three-stage switch fabric with buffered crossbar devices including the following features.

Regarding claim 11, wherein the best effort control means selectively fill said best effort input buffers with best effort data (see Fig. 10, wherein the input buffers, which may include best effort input buffers as shown by Chiussi and mentioned in paragraph [0106] of Dell, in the 1<sup>st</sup> stage block being selectively fills one of the input queues in step 2 of Fig. 10, in the example of the figure, the second queue is currently being selected to be filled).

Regarding claim 14, wherein the best effort control means is further configured to disable best effort requests corresponding to the input of the switching matrix to which the first multiplexer is coupled for a frame during which the guaranteed throughput data is transferred through the switching matrix (see “...at most one bid from each input device, to determine which bids to grant...The bid arbitration...follows the rule...contending bids with lower priority...are rejected in favor of those with higher priority” recited in paragraph [0154], wherein the best effort data is considered lower priority than guaranteed bandwidth data; also see Fig. 18 showing that bids include both inputs and outputs of the crossbar, or switching matrix).

Regarding claim 15, wherein the best effort control means is further configured to disable best effort requests corresponding to the output of the switching matrix to which the guaranteed throughput data is transferred for a frame during which the guaranteed throughput data is transferred through the switching matrix (see "...at most one bid from each input device, to determine which bids to grant...The bid arbitration...follows the rule...contending bids with lower priority...are rejected in favor of those with higher priority" recited in paragraph [0154], wherein the best effort data is considered lower priority than guaranteed bandwidth data; also see Fig. 18 showing that bids include both inputs and outputs of the crossbar, or switching matrix).

Regarding claim 19, wherein the best effort control means is further configured to schedule the best effort data and three steps, wherein the three steps comprises a request step (see "a bid" recited in paragraph [0008]), a grant step (see "arbitrator determines whether to accept (i.e., grant)" recited in paragraph [0008]), and an accept step (see "If a bid is accepted, then a connection is eventually established" recited in paragraph [0008]).

Regarding claim 20, wherein the best effort control means is further configured to schedule the best effort data using multiples of the three steps (see paragraph [0008] explaining how each connection is scheduled using the three step of bid, grant, connect steps; thus multiple bids would be processed by the multiple of the three steps).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Karawai using features, as taught by Chiussi and Moore, in order to ensure that all guaranteed bandwidth flows could be transmitted

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while meeting the resource requirements and in order to provide “bandwidth, throughput, and/or goodput provisioning of multiple TCP flows across shared links” and to obviate “the need for congestion signaling” (see Moore, paragraph [0004]) and in order to provide scheduling based on the QoS (see “Queue Structures, QoS Schedulers” section under paragraph [0105] of Dell).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUTAI KAO whose telephone number is (571)272-9719. The examiner can normally be reached on Monday ~Friday 7:30 AM ~5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571)272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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